SN54190, SN54191, SN54LS190, SN54LS191, SN74190, SN74191, SN74LS190, SN74LS191
Synchronous Up/Down Counters with Down/Up Mode Control
DECEMBER 1972 - REVISED MARCH 1985

- Counts 0-4-2-1 BCD or Binary
- Single Down/Up Count Control Line
- Count Enable Control Input
- Ripple Clock Output for Cascading
- Asynchronously Presetable with Load Control
- Parallel Outputs
- Cascadable for n-Bit Applications

<table>
<thead>
<tr>
<th>TYPE</th>
<th>PROPAGATION DELAY</th>
<th>TYPICAL MAXIMUM FREQUENCY</th>
<th>TYPICAL POWER DISSIPATION</th>
</tr>
</thead>
<tbody>
<tr>
<td>'180, '191</td>
<td>20 ns</td>
<td>25MHz</td>
<td>325mW</td>
</tr>
<tr>
<td>LS190, LS191</td>
<td>20 ns</td>
<td>25MHz</td>
<td>100mW</td>
</tr>
</tbody>
</table>

description

The '190, '180, '191, and '181' are synchronous, reversible up/down counters having a complexity of 58 equivalent gates. The '191 and '181' are 4-bit binary counters and the '190 and '180' are BCD counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple clock) counters.

The outputs of the four master-slave flip-flops are triggered on a low-to-high transition of the clock input if the enable input is low. A high at the enable input inhibits counting. Level changes at the enable input should be made only when the clock input is high. The direction of the count is determined by the level of the down/input. When low, the counter count up and when high, it counts down. A false clock may occur if the down/input changes while the clock is low. A false ripple carry may occur if both the clock and enable are low and the down/input is high during a load pulse.

These counters are fully programmable: that is, the outputs may be preset to either level by placing a low on the load input and entering the desired data at the data inputs. The output will change to agree with the data inputs independently of the level of the clock input. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

The clock, down/up, and load inputs are buffered to lower the drive requirement which significantly reduces the number of clock drivers, etc., required for long parallel words.

Two outputs have been made available to perform the cascading function: ripple clock and maximum/minimum count. The latter output produces a high-level output pulse with a duration approximately equal to one complete cycle of the clock when the counter overflows or underflows. The ripple clock output produces a low-level output pulse equal in width to the low-level portion of the clock input when an overflow or underflow condition exists. The counters can be easily cascaded by feeding the ripple clock output to the enable input of the succeeding counter if parallel clocking is used, or to the clock input if parallel enabling is used. The maximum/minimum count output can be used to accomplish look-ahead for high-speed operation.

Series 54' and 54LS' are characterized for operation over the full military temperature range of -55°C to 125°C; Series 74' and 74LS' are characterized for operation from 0°C to 70°C.

PRODUCTION DATA documents contain information current as of publication date. Prototypes conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

TEXAS INSTRUMENTS
POST OFFICE BOX 14424 * DALLAS, TEXAS 75215
SN54190, SN54191, SN54LS190, SN54LS191, SN74190, SN74191, SN74LS190, SN74LS191
SYNCHRONOUS UP/DOWN COUNTERS WITH DOWN/UP MODE CONTROL

logic symbols†

†These symbols are accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.
Pin numbers shown are for D, J, and N packages.
SN54191, SN54LS191, SN74191, SN74LS191
SYNCHRONOUS UP/DOWN COUNTERS WITH DOWN/UP MODE CONTROL

Pin numbers shown are for D, J, and N packages.
typical load, count, and inhibit sequences

Illustrated below is the following sequence:
1. Load (preset) to BCD seven.
2. Count up to eight, nine (maximum), zero, one, and two.
3. Inhibit.
4. Count down to one, zero (minimum), nine, eight, and seven.
SN54191, SN54LS191, SN74191, SN74LS191
SYNCHRONOUS UP/DOWN COUNTERS WITH DOWN/UP MODE CONTROL

191, 'LS191 BINARY COUNTERS

typical load, count, and inhibit sequences

Illustrated below is the following sequence:
1. Load (preset) to binary thirteen.
2. Count up to fourteen, fifteen (maximum), zero, one, and two.
3. Inhibit.
4. Count down to one, zero (minimum), fifteen, fourteen, and thirteen.

LOAD

DATA INPUTS

CLOCK

D/\U

CTFN

QA

QB

QC

QD

MAX/MIN

REG

13 14 15 0 1 2 2 2 1 0 15 14 13

COUNT UP INHIBIT COUNT DOWN

Texas Instruments
POST OFFICE BOX 655012 - DALLAS, TEXAS 75265
absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC (see Note 1) ........................................ 7 V
Input voltage: SN54\*, SN74\* Circuits ........................................ 5.5 V
SN54LS\*, SN74LS\* Circuits .................................................. 7 V
Operating free-air temperature range: SN54\*, SN54LS\* Circuits .................................................. -55°C to 125°C
SN74\*, SN74LS\* Circuits .................................................. 0°C to 70°C
Storage temperature range .................................................. -65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>VCC</th>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
<th>SN54190, SN54191</th>
<th>SN74190, SN74191</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>4.5</td>
<td>5</td>
</tr>
<tr>
<td>IGH</td>
<td>High-level output current</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>4.75</td>
</tr>
<tr>
<td>IOL</td>
<td>Low level output current</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>16</td>
</tr>
<tr>
<td>IHEE</td>
<td>Input enable current</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td>TWLO</td>
<td>Width of clock input pulse</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>25</td>
</tr>
<tr>
<td>TWLO</td>
<td>Width of load input pulse</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>30</td>
</tr>
<tr>
<td>SD</td>
<td>Setup time</td>
<td>Data, high or low (See Figure 1 and 2)</td>
<td></td>
<td></td>
<td></td>
<td>20</td>
</tr>
<tr>
<td>hold</td>
<td>Date hold time</td>
<td>Load inactive state</td>
<td></td>
<td></td>
<td></td>
<td>20</td>
</tr>
<tr>
<td>TA</td>
<td>Operating free-air temperature</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>-55</td>
</tr>
</tbody>
</table>

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>SN54190, SN54191</th>
<th>SN74190, SN74191</th>
</tr>
</thead>
<tbody>
<tr>
<td>VIL</td>
<td>Low-level input voltage</td>
<td>VCC = MIN</td>
<td>2</td>
</tr>
<tr>
<td>VIL</td>
<td>Low-level input voltage</td>
<td>VCC = MIN</td>
<td>0.8</td>
</tr>
<tr>
<td>IIL</td>
<td>Input high voltage</td>
<td>VCC = MIN, IIL = -12 mA</td>
<td>-1.5</td>
</tr>
<tr>
<td>VOH</td>
<td>High-level output voltage</td>
<td>VCC = MIN, VIL = 0.8 V, IOH = -0.8 mA</td>
<td>2.4</td>
</tr>
<tr>
<td>VOL</td>
<td>Low-level output voltage</td>
<td>VCC = MIN, VIL = 0.8 V, IOL = 16 mA</td>
<td>0.2</td>
</tr>
<tr>
<td>IH</td>
<td>High-level input current at maximum input voltage</td>
<td>VCC = MAX, VIL = 5.5 V</td>
<td>1</td>
</tr>
<tr>
<td>IIL</td>
<td>High-level input current at any input except enable</td>
<td>VCC = MAX, VIL = 2.4 V</td>
<td>40</td>
</tr>
<tr>
<td>IHEE</td>
<td>High-level input current at enable input</td>
<td>VCC = MAX, VIL = 2.4 V</td>
<td>120</td>
</tr>
<tr>
<td>ILE</td>
<td>Low-level input current at any input except enable</td>
<td>VCC = MAX, VIL = 0.4 V</td>
<td>-1.6</td>
</tr>
<tr>
<td>ILE</td>
<td>Low-level input current at enable input</td>
<td>VCC = MAX, VIL = 0.4 V</td>
<td>-4.8</td>
</tr>
<tr>
<td>ISC</td>
<td>Short-circuit output current</td>
<td>VCC = MAX</td>
<td>-20</td>
</tr>
<tr>
<td>ICC</td>
<td>Supply current</td>
<td>VCC = MAX, See Note 2</td>
<td>65</td>
</tr>
</tbody>
</table>

1 For conditions shown as MAX or MIN, use appropriate value specified under recommended operating conditions.
2 All typical values are at VCC = 5 V, TA = 25°C.
3 Not more than one output should be shorted at a time.

NOTE 2: ICC is measured with all inputs grounded and all outputs open.
SN54190, SN54191, SN74190, SN74191
SYNCHRONOUS UP/DOWN COUNTERS WITH DOWN/UP MODE CONTROL

switching characteristics, $V_{CC} = 5$ V, $T_A = 25^\circ$C

<table>
<thead>
<tr>
<th>PARAMETER†</th>
<th>FROM (INPUT)</th>
<th>TO (OUTPUT)</th>
<th>TEST CONDITIONS</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_{PLH}$</td>
<td>Load</td>
<td>$Q_A, Q_B, Q_C, Q_D$</td>
<td>$C_L = 16$ µF, $R_L = 400$ Ω, See Figures 1 and 3 thru 7</td>
</tr>
<tr>
<td>$t_{PHL}$</td>
<td>Data A, B, C, D</td>
<td>$Q_A, Q_B, Q_C, Q_D$</td>
<td></td>
</tr>
<tr>
<td>$t_{PLH}$</td>
<td>CLK</td>
<td>$R_{CO}$</td>
<td></td>
</tr>
<tr>
<td>$t_{PHL}$</td>
<td>CLK</td>
<td>$Q_A, Q_B, Q_C, Q_D$</td>
<td></td>
</tr>
<tr>
<td>$t_{PLH}$</td>
<td>CLK</td>
<td>Max/Min</td>
<td></td>
</tr>
<tr>
<td>$t_{PHL}$</td>
<td>$D/\bar{D}$</td>
<td>$R_{CO}$</td>
<td></td>
</tr>
<tr>
<td>$t_{PHL}$</td>
<td>$D/\bar{D}$</td>
<td>Max/Min</td>
<td></td>
</tr>
</tbody>
</table>

†$f_{max} = $ maximum clock frequency  
$\tau_{PLH} = $ propagation delay time, low-to-high-level output  
$\tau_{PHL} = $ propagation delay time, high-to-low-level output

schematics of inputs and outputs

**EQUIVALENT OF EACH INPUT**

![Equivalent of each input](image)

Enable input: $R_{eq} = 1.3 \Omega$ NOM  
All other inputs: $R_{eq} = 6 \times 10^3$ NOM

**TYPICAL OF ALL OUTPUTS**

![Typical of all outputs](image)

Texas Instruments
POST OFFICE BOX 302602 - DALLAS, TEXAS 75269
# SN54LS190, SN54LS191, SN74LS190, SN74LS191
## SYNCHRONOUS UP/DOWN COUNTERS WITH DOWN/UP MODE CONTROL

### Recommended Operating Conditions

<table>
<thead>
<tr>
<th>Parameter</th>
<th>SN54LS190</th>
<th>SN74LS190</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{CC} ) (Supply voltage)</td>
<td>4.5 V, 5.5 V</td>
<td>4.75 V, 5.5 V</td>
</tr>
<tr>
<td>( I_{OH} ) (High-level output current)</td>
<td>-0.4 mA</td>
<td>-0.4 mA</td>
</tr>
<tr>
<td>( I_{OL} ) (Low-level output current)</td>
<td>-4 mA</td>
<td>8 mA</td>
</tr>
<tr>
<td>( f_{clock} ) (Clock frequency)</td>
<td>0 20 Hz</td>
<td>0 20 MHz</td>
</tr>
<tr>
<td>( t_{W(\text{max})} ) (Width of clock input pulse)</td>
<td>25 ns</td>
<td>25 ns</td>
</tr>
<tr>
<td>( t_{W(L)} ) (Width of load input pulse)</td>
<td>35 ns</td>
<td>35 ns</td>
</tr>
<tr>
<td>( t_{DDU} ) (Data setup time)</td>
<td>20 ns</td>
<td>20 ns</td>
</tr>
<tr>
<td>( t_{DDH} ) (Data hold time)</td>
<td>5 ns</td>
<td>5 ns</td>
</tr>
<tr>
<td>( t_{E} ) (Enable hold time)</td>
<td>0 ns</td>
<td>0 ns</td>
</tr>
<tr>
<td>( t_{QEN} ) (Count enable time)</td>
<td>40 ns</td>
<td>40 ns</td>
</tr>
<tr>
<td>( T_{A} ) (Operating free-air temperature)</td>
<td>-55 °C to 125 °C</td>
<td>0 °C to 70 °C</td>
</tr>
</tbody>
</table>

### Electrical Characteristics over Recommended Operating Free-Air Temperature Range (Unless Otherwise Noted)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Test Conditions</th>
<th>SN54LS190</th>
<th>SN54LS191</th>
<th>SN74LS190</th>
<th>SN74LS191</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{IH} ) (High-level input voltage)</td>
<td>2 V</td>
<td>2 V</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{IL} ) (Low-level input voltage)</td>
<td>0.7 V</td>
<td>0.8 V</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{IL} ) (Input clamp voltage)</td>
<td>( V_{CC} = \text{MIN}, ; I_{IL} = -18 \text{ mA} )</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{OH} ) (High-level output voltage)</td>
<td>( V_{CC} = \text{MIN}, ; V_{IH} = 2 \text{ V} )</td>
<td>2.5 V</td>
<td>3.4 V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{OL} ) (Low-level output voltage)</td>
<td>( V_{CC} = \text{MIN}, ; V_{IL} = -400 \text{ \mu A} )</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( I_{H} ) (High-level input current at maximum input voltage)</td>
<td>( V_{CC} = \text{MAX}, ; V_{I} = 7 \text{ V} )</td>
<td>0.3 mA</td>
<td>0.3 mA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( I_{L} ) (Low-level input current)</td>
<td>( V_{CC} = \text{MAX}, ; V_{I} = 2.7 \text{ V} )</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( I_{Q} ) (Short-circuit output current)</td>
<td>( V_{CC} = \text{MAX} )</td>
<td>-20 mA</td>
<td>-100 mA</td>
<td>-20 mA</td>
<td>-100 mA</td>
</tr>
<tr>
<td>( I_{CC} ) (Supply current)</td>
<td>( V_{CC} = \text{MAX} )</td>
<td>20 mA</td>
<td>38 mA</td>
<td>20 mA</td>
<td>38 mA</td>
</tr>
</tbody>
</table>

1. For conditions shown as MAX or MIN, use appropriate value specified under recommended operating conditions for the applicable device type.
2. All typical values are at \( V_{CC} = 5 \text{ V}, \; T_{A} = 25^\circ \text{C} \).
3. Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

**NOTES:**
1. \( I_{CC} \) is measured with all inputs grounded and all outputs open.
2. Minimum count enable time is the interval immediately preceding the rising edge of the clock pulse during which interval the count enable input must be low to ensure counting.

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**Texas Instruments**

POST OFFICE BOX 655012 • DALLAS, TEXAS 75260
SN54LS190, SN54LS191, SN74LS190, SN74LS191
Synchronous Up/Down Counters with Down/Up Mode Control

Switching Characteristics, \( V_{CC} = 5 \text{ V}, T_A = 25^\circ \text{C} \)

<table>
<thead>
<tr>
<th>PARAMETER ( f )</th>
<th>FROM (INPUT) ( f )</th>
<th>TO (OUTPUT) ( f )</th>
<th>TEST CONDITIONS</th>
<th>( 'LS190, 'LS191 ) Min</th>
<th>Typ</th>
<th>Max</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( f_{\text{min}} )</td>
<td>( \text{Load} )</td>
<td>( QA, QB, QC, QD )</td>
<td>( C_L = 15 \text{ pF}, R_L = 2 \text{ k} \Omega )</td>
<td>20</td>
<td>22</td>
<td>25</td>
<td>( \mu \text{sec} )</td>
</tr>
<tr>
<td>( t_{\text{PLH}} )</td>
<td>( \text{Data A, B, C, D} )</td>
<td>( QA, QB, QC, QD )</td>
<td>( \text{See Figures 1 and 3 thru 7} )</td>
<td>22</td>
<td>23</td>
<td>25</td>
<td>( \mu \text{sec} )</td>
</tr>
<tr>
<td>( t_{\text{PHL}} )</td>
<td>( \text{CLK} )</td>
<td>( QD )</td>
<td></td>
<td>20</td>
<td>21</td>
<td>25</td>
<td>( \mu \text{sec} )</td>
</tr>
<tr>
<td>( t_{\text{PLH}} )</td>
<td>( \text{CLK} )</td>
<td>( QA, QB, QC, QD )</td>
<td></td>
<td>21</td>
<td>22</td>
<td>25</td>
<td>( \mu \text{sec} )</td>
</tr>
<tr>
<td>( t_{\text{PHL}} )</td>
<td>( \text{CLK} )</td>
<td>( \text{Max/Min} )</td>
<td></td>
<td>21</td>
<td>22</td>
<td>25</td>
<td>( \mu \text{sec} )</td>
</tr>
<tr>
<td>( t_{\text{PLH}} )</td>
<td>( \text{D/\bar{D}} )</td>
<td>( \text{RCD} )</td>
<td></td>
<td>21</td>
<td>22</td>
<td>25</td>
<td>( \mu \text{sec} )</td>
</tr>
<tr>
<td>( t_{\text{PHL}} )</td>
<td>( \text{D/\bar{D}} )</td>
<td>( \text{Max/Min} )</td>
<td></td>
<td>21</td>
<td>22</td>
<td>25</td>
<td>( \mu \text{sec} )</td>
</tr>
<tr>
<td>( t_{\text{PHL}} )</td>
<td>( \text{CTEN} )</td>
<td>( \text{RCD} )</td>
<td></td>
<td>21</td>
<td>22</td>
<td>25</td>
<td>( \mu \text{sec} )</td>
</tr>
</tbody>
</table>

\( f_{\text{MAX}} = \text{maximum clock frequency} \)
\( t_{\text{PLH}} = \text{propagation delay time, low-to-high-level output} \)
\( t_{\text{PHL}} = \text{propagation delay time, high-to-low-level output} \)

Schematics of Inputs and Outputs

**Equivalent of Each Input**

![Equivalent of Each Input Diagram]

Frakle input: \( R_{eq} = 8.93 \Omega \text{ NOM} \)
Load input: \( R_{eq} = 25 \text{ k} \Omega \text{ NOM} \)
All other inputs: \( R_{eq} = 17 \text{ k} \Omega \text{ NOM} \)

**Typical of All Outputs**

![Typical of All Outputs Diagram]

Texas Instruments
POST OFFICE BOX 655303 * DALLAS, TEXAS 75265
PARAMETER MEASUREMENT INFORMATION

OUTPUT VCC

MAX/MIN.
RIPPLE CLOCK,
Qa, Qb, Qc, OR Qd

C_L = 15 pF
(SEE NOTE A)

(SEE NOTE B)

FIGURE 1—LOAD CIRCUIT
FOR SWITCHING TIME MEASUREMENT

DATA INPUT
(SEE NOTE C)

< 10 ns
10% Vref
90%
< 10 ns
90% Vref
10%
< 10 ns
10%

LOAD INPUT
(SEE NOTE C)

< 10 ns
10% Vref
90%
< 10 ns
90% Vref
10%
< 10 ns
10%

FIGURE 2 DATA SETUP TIME VOLTAGE WAVEFORMS

< 10 ns

INPUT
(SEE NOTE C)

< 10 ns
10% Vref
90%
< 10 ns
90% Vref
10%
< 10 ns
10%

NONINVERTING OUTPUT

Vref

INVERTING OUTPUT

Vref

See waveform sequences in figures 4 through 7 for propagation times from a specific input to a specific output. For simplification, pulse rise times, reference levels, etc., have not been shown in figures 4 through 7.

FIGURE 3—GENERAL VOLTAGE WAVEFORMS FOR PROPAGATION TIMES

NOTES:
A. C_L includes probe and jig capacitance.
B. All diodes are 1N3904 or equivalent.
C. The input pulses are supplied by generators having the following characteristics: Z_out = 50 Ω, duty cycle ≤ 60%, PRF ≤ 1 MHz.
D. V_ref = 1.5 V for '190 and '191; 1.3 V for 'LS190 and 'LS191.
PARAMETER MEASUREMENT INFORMATION (continued)

LOAD

ANY DATA INPUT

CORRESPONDING Q OUTPUT

NOTE E: Conditions on other inputs are irrelevant.

FIGURE 4—LOAD TO OUTPUT AND DATA TO OUTPUT

LOAD

D/U

CLOCK

EN

RCO

MAX/MIN

NOTE F: All data inputs are low.

FIGURE 5—ENABLE TO RIPPLE CLOCK, CLOCK TO RIPPLE CLOCK, DOWN/UP TO RIPPLE CLOCK, AND DOWN/UP TO MAX/MIN
PARAMETER MEASUREMENT INFORMATION (continued)

switching characteristics (continued)

**Figure 6**-Clock to Output

**Figure 7**-Clock to Max/Min

**NOTES:**
1. To test $Q_A$, $Q_B$, and $Q_C$ outputs of '190 and 'LS190: Data inputs A, B, and C are shown by the solid line. Data input D is shown by the dashed line.
2. To test $Q_D$ output of '190 and 'LS190: Data inputs A and D are shown by the solid line. Data inputs B and C are held at the low logic level.
3. To test $Q_A$, $Q_B$, $Q_C$, and $Q_D$ outputs of '101 and 'LS191: All four data inputs are shown by the solid line.

**NOTE J:** Data inputs B and C are shown by the dashed line for the '190 and 'LS190 and the solid line for the '101 and 'LS191: Data input D is shown by the solid line for both devices.
IMPORTANT NOTICE

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